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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,596	09/09/2003	Gregory J. Smith	50019.252US01	1922

23552 7590 12/10/2004

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EXAMINER	
RILEY, SHAWN	
ART UNIT	**PAPER NUMBER**
2838	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,596	SMITH ET AL.	
	Examiner	Art Unit	
	Shawn Riley	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-18* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," "What is disclosed", "The invention relates to", "Methods and apparatus are provided", "**The present invention shows**", "According to the invention", "The objective of the invention", or like phases, etc. Correction is required. See MPEP § 608.01(b).

Claim Objections

2. Claims 1, 9 and 14 are objected to under 37 C.F.R. 1.75(a) because of the following informalities: In claim 1;

at third line from bottom, repeat of "a". Appropriate correction is required.

In claim 9,

The term "*a second node*" is confusing and is taken as a first node since it is not clear that there is a first node. Appropriate correction is required.

In claim 14;

The apparatus of Claim 9, further comprising an amplifier having an input coupled to an emitter node, an input coupled to a collector node and an output coupled to a gate; and a transistor coupled to the emitter node and the second node;

This paragraph is not clear, first of all there is no drawing or suggestion that the amplifier (taken for examination purposes as 125) has any input connected to an emitter since a FET is shown (M3) –in which case terminology such as source/drain would be appropriate. For examination purposes the emitter is taken to be a source. What does applicant mean by 'the second node'. Where is the first/second (see objection to claim 9)? Further, this claim appears to be incomplete because of the punctuation and is therefore doubly difficult to follow. Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4, 6-9, and 15-18 are rejected under 35 U.S.C. §102(b) as being fully anticipated by Takuma (U.S. Patent 4,810,948). Takuma shows,[1] (in, e.g., the(ir) figure 2 and corresponding disclosure)

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1 Note claims will be addressed individually and the material in parentheses are the examiner's annotated comments. Further unless needed for clarity reasons, recited limitation(s), will be annotated only upon their first occurrence. Annotated claims begin with the phrase "As to claim". Claims that are not annotated are seen as having already had the invention(s) addressed previously in an annotated claim. Bolded words/phrases indicate rejected material based 112 paragraph rejections. Underlined words/phrases indicate objected to material. For method claims, note that under MPEP 2112.02, the principles of inherency, if a prior art device, in its normal and usual operation, would necessarily perform the method claimed, then the method claimed will be considered to be anticipated by the prior art device. When the prior art device is the same as a device described in the specification for carrying out the claimed method, it can be assumed the device will inherently perform the claimed process. In re King, 801 F.2d 1324, 231 USPQ 136 (Fed. Cir. 1986). Therefore the previous rejections based on the apparatus

As to claim 1;

A circuit for current regulation, comprising:

a regulation circuit (see, e.g., figure 2 and description starting at column 1 lines 50 through 63, including OUTPUT CONTROL TRANSISTOR) coupled to a power supply (INPUT) and configured to generate a regulated current to a load (OUTPUT);

a mode circuit (including MULTIPLEXER/OP AMP/) having an input coupled to a control signal (n) and an output (into OP AMP) configured to generate a mode signal relating to an open mode (where the full value of the input/output would be substantially unchanged, see, e.g., column 2 lines 4-11 discussing high range of output, i.e., 10 volts) and a linear mode (specifically 1.5V +/- .2V also at column 2 line 6) associated with the regulation circuit;

a comparator (OP AMP) having an input coupled to a signal relating to a voltage associated with the regulation circuit (i.e., coupled to REFERENCE VOLTAGE GENERATOR CIRCUIT) an input coupled to the mode signal (output of MULTIPLEXER) and configured to compare the mode signal and the signal relating to the voltage;

a switch circuit (OUTPUT CONTROL TRANSISTOR) coupling an output of the comparator to a linear mode control node when the circuit is operating in the linear mode and to an open mode control node when the circuit is operating in the open mode (see above discussion in the third sub paragraph relating to the mode circuit); and *a*

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will not be repeated.

a control circuit (DATA REGISTER/WE/BUS) coupled to the mode circuit and configured to generate a control signal used in controlling the mode circuit.

As to claim 2;

The circuit of Claim 1, wherein the regulation circuit is a transistor (OUTPUT CONTROL TRANSISTOR) that operates one of the linear control mode and the open mode.

As to claim 3;

The circuit of Claim 1, wherein the mode circuit further comprises a multiplexer (MULTIPLEXER) and a resistor ladder (R1-R(2n-1)) that is coupled to a reference signal (OUTPUT).

As to claim 4;

The circuit of Claim 3, wherein the multiplexer is coupled to the control signal and arranged to select a tap point associated with the resistor ladder (definition of how multiplexers work, also see column 1 lines 56-60).

As to claim 6;

The circuit of Claim 1, wherein the switch circuit is configured to switch from the open mode to the linear control mode when the regulation circuit is in a overloaded state (as with all regulators, as the output rises the regulation-i.e., the pass transistor—is more tightly controlled, squeezed into the off position and therefor brought into the 'linear mode').

As to claim 7;

The circuit of claim 6, wherein the switch circuit is configured to switch back to the open mode (see explanation in claim 6).

As to claim 8;

The circuit of Claim 4, wherein the control (this is done through address inputs, see column 1 lines 60-69) generates the control signal such that the multiplexer selects different tap points while the circuit operates in the linear mode.

> 9.An apparatus for current regulation, comprising: a transistor configured to operate in a linear control mode and an open mode*; a second node* that is coupled to a signal that is proportional to a voltage across the transistor configured to operate in the linear control mode and the open mode; a comparator having an input coupled to a mode signal, an input coupled to the second node, and arranged to compare the inputs and output an output signal; a switch circuit coupled to the output signal and configured to couple the output signal to a linear mode node when the circuit is operating in the linear control mode; and to the open mode node when the circuit is operating in the open mode; a control circuit coupled to the linear mode node and to the open mode node and configured to generate a control signal; and a mode circuit coupled to the control signal and configured to output the mode signal in response to the control signal.
>
> 15. A method for current regulation of a circuit, comprising; comparing a signal to an overload signal when in an open mode; determining when a regulation circuit is overloaded, changing to a linear mode when overloaded; and when the circuit is in the linear mode: adjusting a multiplexer to select a tap point in a resistor ladder, and comparing the signal to a signal associated with the selected tap point using the same comparator that compared the signal to the overload signal.
> 16. The method of Claim 15, further comprising switching back to the open mode.
> 17. An apparatus for current regulation, comprising: means for comparing a signal to an overload signal when in an open mode; means for determining when a regulation circuit is overloaded when the circuit is operating in the open mode; means for changing to a linear mode when the regulation circuit is overloaded; and when the circuit is operating in the linear mode: means for adjusting a multiplexer to select a tap point in a resistor ladder; and means for comparing the signal to a signal associated

with the selected tap point using the same comparator that compared the signal to the overload signal.
18. The apparatus of Claim 17, further comprising means for switching the circuit back to the open mode.

Claim Rejections - 35 U.S.C. § 103

3. The following is a quotation of 35 U.S.C. § 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

4. Claims 5, and 10 (and therefore 11-13) are rejected under 35 U.S.C. § 103 as being unpatentable over Takuma (U.S. Patent 4,810,948). The Takuma reference discloses the limitations of the invention as claimed as described above. However, Takuma does not show the transistor being an p-n-p type as recited in claims 5 and 10. It would have been obvious at the time the invention was made to utilize p-n-p type into the circuit of Takuma for the reason of providing a variable resistance. That is, many varieties of bipolar transistors and FETs exist and are designed for different environments. For instance, some bipolar transistors are able to withstand a higher reverse breakdown voltage which is generally traded for a slower switching speed. These various types of similar transistors (e.g., pnp and npn bipolar transistors with wider channels, different amounts of doping, or MOSFETs, IGBTs, etc.) have in common the use of providing a desired transresistance function (by current for bipolars). Accordingly, it would have been obvious to one of ordinary skill in the art to replace generic pass transistors with the bipolar pnp given the expected working environment in view of their closely related theoretical basis (all pass transistors in general) and the resulting expectation of a similar result, i.e., providing a current pass function by current for a bipolar (or likewise providing a current pass function by voltage for an FET).

11. The apparatus of Claim 10, wherein the mode circuit further comprises a multiplexer coupled to the control signal and a resistor ladder that is coupled to the multiplexer.
12. The apparatus of Claim 10, wherein the mode circuit outputs a constant signal when the circuit is in the open mode.
13. The apparatus of Claim 11, wherein the multiplexer selects tap points in the resistor ladder when the circuit is in the linear mode.

Allowable Subject Matter

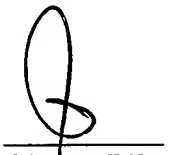
5. Claim 14 would be allowable if rewritten or amended to overcome the objection.

6. As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and section 707.07(a) of the M.P.E.P.

Conclusion

Any inquiry from other than the applicant/attorney of record concerning this communication or earlier communications from the Examiner should be directed to the Patent Electronic Business Center (EBC) at 1.866.217.9197. Any inquiry from a member of the press concerning this communication or earlier communications from the Examiner or the application should be directed to the Office of Public Affairs at 703.305.8341. Any inquiry from the applicant or an attorney of record concerning this communication or earlier communications from the Examiner should be directed to Examiner Riley whose telephone number is 571.272.2083. The Examiner can normally be reached Monday through Thursday from 7:30-6:00 p.m. Eastern Standard Time. The Examiner's Supervisor is Mike Sherry who can be reached at 571.272.2084. Any inquiry about a case's location, retrieval of a case, or receipt of an amendment into a case or information regarding sent correspondence to a case **should be directed to 2800's Customer Service Center** at 571.272.2815. Any papers to be sent by fax MUST BE sent to fax number 703.872.9306. Any inquiry of a general nature of this application should be **directed to the Group receptionist** whose telephone number is 571.272.2800. Status information of cases may be found at http://pair-direct.uspto.gov wherein unpublished application information is found through private PAIR and published application information is found through public PAIR. Further help on using the PAIR system is available at 1.866.217.9197 (Electronic Business Center).

December 04



Shawn Riley
Primary Examiner